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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/527,761	03/17/2000	Brian C. Barker	BU9-99-157	3261
30678	7590	07/07/2005	EXAMINER	
CONNOLLY BOVE LODGE & HUTZ LLP SUITE 800 1990 M STREET NW WASHINGTON, DC 20036-3425			LEE, SEUNG H	
			ART UNIT	PAPER NUMBER
			2876	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

09/527,761

Applicant(s)

BARKER ET AL

Examiner

Seung H. Lee

Art Unit

2876

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 06 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-67 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-26, 28-35, 37-46 and 51-67 is/are rejected.
- 7) ☒ Claim(s) 27, 36 and 47-50 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. Receipt is acknowledged of the Appeal Brief filed on 06 October 2003, which has been entered in the file.

#### ***Response to Appeal Brief***

2. Applicant's Appeal Brief with respect to claims 1-67 have been considered but are moot in view of the new ground(s) of rejection.

The Bacchi teaches that the semiconductor wafers are marked with the identifying information to track during production of integrated circuits on the wafer wherein the identifying marks known as scribe marks comprises a series of characters, barcodes, or two dimensional codes (see col. 1, lines 15-20). Also, the White reference teaches the coating layer for coating the indicia located on the wafer as discussed in paragraph 9.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

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4. Claims 1, 2, 6, 9, 13, 22, 37, 40, 43-46, 51, 54, 55, 58, 60, 63, and 64 rejected under 35 U.S.C. 102(e) as being anticipated by Bacchi et al. (US 5,894,348, of the record)(hereinafter referred to as 'Bacchi').

Bacchi teaches that semiconductor wafers are marked with identifying information to facilitate in-process tracking during their production (col. 1, lines 15-28) wherein a plurality of pits or scribe markers (18) used as identifying mark for tracking during manufacturing of integrated circuits using the wafers, a plurality of pits or scribe markers (18) shape in circle, wherein the markers are located on a front side of the semiconductor wafer (20) in which the pits are arranged in digital information-providing pattern (i.e., alphanumeric characters) wherein a scribe mark reader (10) reads the pits during production process using diode array (16), and the adequate or detectable contrast between the background and the image of the mark, the markers are readable by a reader's eye, the pits (28) are oriented differently defined by each of an associated axis (see Figs. 1, 3-5; col. 1, line 15- col. 2, line 27; col. 4, line 13-col. 8, line 52).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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6. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bacchi in view of Moh et al (US 6,214,250, of the record)(hereinafter referred to as 'Moh') and Huang et al (US 5,330,924)(hereinafter referred to as 'Huang').

The teachings of Bacchi have been discussed above.

Although, Bacchi teaches that the pits on the semiconductor wafer contrast with surrounding portion of wafer, they fail to teach or fairly suggest that the pits are arranged in the an ion implant region to provide a contrast.

However, Moh teaches of forming code pattern according to contrast of layers resulted in the depth of codes (see fig. 4; col. 13, line 32- col. 14, line 4), and Huang teaches that the ion implantation is used to characterize the wafer (see Figs. 7 and 8; col. 4, lines 36-54).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the well-known method of ion implant as taught by Huang and forming code pattern using layers having contrast as taught by Moh with the method of composite label as taught by Bacchi in order to provide the conductance to wafer. Moreover, such modification also provides clear reading of the code on the wafer optically since the top layer is discernible from the base layer.

7. Claims 7, 8, 10; 16, 21, 28-30, 33-35, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bacchi in view of Duncan et al (US 4,585,931, of the record)(hereinafter referred to as 'Duncan').

The teachings of Bacchi have been discussed above.

In addition to the teachings of Bacchi as discussed above, he also teaches a character is consist of a plurality of pits (28) having a space between each pits (see Fig. 5, col. 4, line 13-24).

However, Bacchi teaches the pits are arranged in information providing pattern, he fails to teach or fairly suggest that the pattern have long and short pits.

Duncan teaches that the bar codes on the wafer are varying by width and height or a first shape and a second shape and the light striking spaces (21) between the pits (15 and 18) form the interference fringes in which defines by the depth of the space (21) and the rays of light are reflected with a phase change (II) (39, 39', 39", and 39''') wherein the reflected beam does not reaches the sensing device (39) considered as non-reflected (see Figs. 1-3; col. 3, lines 49-60; col. 5, line 21-47).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Duncan to the teachings of Bacchi in order to improve the readability of the information mark of the wafer by scattering the rays of light onto the surface of the wafer. Although, Bacchi as modified by Duncan and Young fail to particularly teach or fairly suggest that the height and width of the pits and the distance between each pits, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Duncan to the teachings of Bacchi, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

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8. Claims 11, 12, 17-19, and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bacchi in view of Young et al (US 5,792,566, of the record)(hereinafter referred to as 'Young').

The teachings of Bacchi have been discussed above.

Although, Bacchi teaches that the pits are on the semiconductor wafer, they fail to teach or fairly suggest that the pits are perpendicular to a top surface and a bottom surface of the wafer.

However, Young teaches the pit (172) is grooved on the side surface of the wafer extending from the front surface of the wafer to a back surface of the wafer when the wafer of Fig.1 is cut horizontally wherein the pit is perpendicular to a top surface and a bottom surface of the wafer (see Fig. 1-3; col. 2, line 55- col. 4, line 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Young to the teachings of Bacchi in order to align/stack the wafers by matching the information mark or pits of wafers. Moreover, such modification would provide the faster processing means by aligning/stacking the wafers based on the pits provided thereon which is in the position for next processing steps. Although, Bacchi as modified by Young fail to particularly teach that the groove is curved on the boule, it would have been an obvious design variation well within the ordinary skill in the art failing to provide any unexpected results for aligning/stacking the wafer by the matching location of the pits of wafer.

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9. Claims 14 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bacchi in view of Yano et al (US 6,268,641, of the record)(hereinafter referred to as 'Yano').

The teachings of Bacchi have been discussed above.

Although, Bacchi teaches that the pits on the semiconductor wafer, they fail to teach or fairly suggest that a laser reading device is reading information.

However, Yano teaches the laser-reading device can be used for reading of the identification mark (16) on the wafer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the conventional laser reading device of the Yano for the reader of the Bacchi in order to improve a readability of the information marks or pits means wherein the information marks or pits are canned precisely and accurately using the laser reading device.

10. Claims 15 and 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bacchi in view of White et al. (US 5,949,584)(hereinafter referred to as 'White').

The teachings of Bacchi have been discussed above.

Although, Bacchi teaches that the pits on the semiconductor wafer, they fail to teach or fairly suggest that the pits is coated.

However, White teaches the wafer (14) having an indicia (30) wherein the wafer is coated with a coating layer (17) (see figs. 13-15; col. 14, line 57- col. 15, line 24).



It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings White to the teachings of Bacchi in order to prevent/reduce the wear and tear-off of the surface of the wafer by coating the surface of the wafer. Moreover, such modification would provide the clear reading of the pits since the coating of the wafer surface prevent dust materials from resting within the pits.

11. Claims 20, 31, 32, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bacchi in view of Iwai (US 4,418,567, of the record).

The teachings of Bacchi have been discussed above.

Although, Bacchi teaches that the pits on the semiconductor wafer, they fail to teach or fairly suggest that the pits having a location reference information.

However, Iwai teaches that a location mark (114) providing the location information and information marks (116a, 116b, and 116c) providing the wafer's information on the curved sidewalls (see Figs. 9 and 11; col. 7, lines 6-24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings Brown to the teachings of Bacchi in order to an easier recognition of the information means the operator(s) can verify/acknowledge the information written on the wafer without using particular device to decode the information thereon the wafer. Moreover, such modification would provide an automated processing, that is, the operator(s) or computer can be instructed the processing procedure by decoding/reading the information marks.

12. Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bacchi as modified by Duncan, and further in view of Young et al (US 5,792,566, of the record)(hereinafter referred to as 'Young').

The teachings of Bacchi/Duncan have been discussed above.

Although, Bacchi/Duncan teach that the pits are on the semiconductor wafer, they fail to teach or fairly suggest that the pits are arranged the back surface of the wafer.

However, Young teaches the pit (172) is grooved on the side surface of the wafer extending from the front surface of the wafer to a back surface of the wafer when the wafer of Fig.1 is cut horizontally wherein the pit is perpendicular to a top surface and a bottom surface of the wafer (see Fig. 1-3; col. 2, line 55- col. 4, line 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Young to the teachings of Bacchi/Duncan in order to improved and enhanced procedure of reading operation means wherein aligning/stacking of the wafers by matching the information mark or pits of wafers located on the back surface of the wafer would expedite the reading processing since the reader can read the information or pits from any given position.

13. Claim 53 rejected under 35 U.S.C. 103(a) as being unpatentable over Bacchi in view of Makinouchi et al (US 4,958,082, of the record)(hereinafter referred to as 'Makinouchi').

The teachings of Bacchi have been discussed above.

Although, Bacchi teaches that the reading device for reading the pits on the semiconductor wafer, they fail to teach or fairly suggest that the reading device comprises an interferometer.

However, Makinouchi teaches the position of wafer (2) is detected by the interferometer (2) (see Figs. 1 and 2; col. col. 1, lines 12-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings Makinouchi to the teachings of Bacchi in order to an improved and an enhanced means for detecting the orientation of the wafer automatically using the interferometer. Moreover, such modification would speed-up the reading process of the information written on the wafer since the reading device cane be focus on targets area using the interferometer.

14. Claim 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bacchi in view of Wen (US 5,834,819).

The teachings of Bacchi have been discussed above.

Although, Bacchi teaches that the pits are arranged on the semiconductor wafer, he fails to teach or fairly suggest that the pattern of pits is a quaternary-coded pattern having at least three different shapes.

However, Wen teaches the quaternary code is used to encode the data (see Figs. 3A-3H; col. 5, lines 22-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the well-known the quaternary code system as taught by Wen to the teachings of Bacchi in order to increase the storage capacity since the quaternary code can store more information than 1 or 2 dimensional bar code.

15. Claims 56, 57, 61, and 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bacchi in view of Zhang (US 5,245,165).

The teachings of Bacchi have been discussed above.

Although, Bacchi teaches that the pits are arranged on the semiconductor wafer, he fails to teach or fairly suggest that the pattern of pits is comprised at least three different shapes.

However, Zhang teaches a glyph code having at least three different shapes (see Fig. 3; col. 2, lines 3-28; col. 3, lines 7-24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Zhang to the teachings of Bacchi in order to increase the storage capacity using the glyph code wherein the glyph code has a multiple shape representing the different values respectively. Although, Bacchi as modified by Zhang fail to particularly teach that the pits can have different shape including a circle, an oval, and a rectangular. However, it would have been an obvious design variation well within the ordinary skill in the art failing to provide any unexpected results for choosing/designing the shape of the pits to increase capacity for storing information therein.

16. Claims 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bacchi in view of Grandia et al (US 4,084,354)(hereinafter referred to as 'Grandia').

The teachings of Bacchi have been discussed above.

Although, Bacchi teaches that the pits are arranged on the semiconductor wafer, he fails to teach or fairly suggest that the wafer boule having a sequence start notch along a longitudinal surface of boule and a helically shaped sequence notches along a longitudinal surface of boule.

However, Grandia teaches a wafer boule having the sequence start notches (44) along a longitudinal surface of boule and a helically shaped sequence notches (10) along a longitudinal surface of boule (see Figs. 1A and 4A; col. 1, lines 12-60; col. 3, lines 45-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Grandia to the teachings of Bacchi in order to provide an improved and an enhanced cutting means the notches of wafer boule provide an crystallographic orientation of the wafer boule to align with cutting blade during the slicing operation. Although, Bacchi as modified by Grandia fail to particularly teach that the sequence start notches and a helically shaped sequence notches are arranged onto same wafer boule, it would have been an obvious design variation well within the ordinary skill in the art failing to provide any unexpected results for incorporating the two different notches type as taught by Grandia.

***Allowable Subject Matter***

17. Claims 27, 36, and 47-50 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. The following is a statement of reasons for the indication of allowable subject matter:


Although, the best prior art of record to Bacchi, Duncan, Young, Yano, Brown, Iwai, Kakinouchi, and Moh teaches the wafer comprising a plurality of pits for providing information therewith. However, Bacchi, Duncan, Young, Yano, Brown, Iwai, Kakinouchi, and Moh taken alone or in combination of other references, fail to specifically teach or fairly suggest that each group of pits includes a machine-readable set of spaces for pits and each space comprising 2 column each comprising 32 pits, the pits are coated with sapphire or silicon carbide, the pits are formed during wafer processing to record information about the processing, the pits previously formed are altered/invalidated, reading pits formed during processing and using the information read to determined a subsequent processing parameter as set forth in the claim.

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seung H. Lee whose telephone number is (571) 272-2401. The examiner can normally be reached on Monday-Friday, 7:30 AM- 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (571) 272-2398. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
Seung H Lee  
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